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EXAMINER	
MCCOMMAS, STUART S	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,379	CHILDS ET AL.	
	Examiner	Art Unit	
	STUART MCCOMMAS	4115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-13* is/are rejected.

7)☒ Claim(s) *5,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 5 and 8 are objected to because of the following informalities: The claims fail to specifically list which claims they are dependent on. Appropriate correction is required.

Claims 7-8 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, claims 7-8 have not been further treated on the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,2 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Sanford et al. (United States Patent 6,734,636), hereinafter referenced as Sanford.

Regarding claim 1, Sanford discloses an active matrix electroluminescent display device comprising an array of display pixels, each pixel comprising: an electroluminescent display element; an amorphous silicon or microcrystalline silicon first drive NMOS transistor connected between the anode of the display element and a power supply line; a storage capacitor between the anode of the display.element and

the gate of the first drive transistor; and an amorphous silicon or microcrystalline silicon second drive NMOS transistor for supplying a holding voltage to the anode of the display element. Specifically Sanford discloses an OLED display with pixels where each pixel comprises:

an electroluminescent display element or OLED 320 exhibited in figure 3;

an amorphous silicon drive NFET Q303 connected between the anode of the OLED 320 and a power supply line exhibited in figure 3 and disclosed in column 1 lines 13-40.

a storage capacitor CS310 between the anode of the OLED 320 and the gate of the first drive transistor Q303 exhibited in figure 3;

an amorphous silicon drive NFET Q302 for supplying a holding voltage to the anode of the OLED 320 exhibited in figure 3 and disclosed in column 1 lines 13-40 and in column 6 lines 10-67.

Regarding claim 2, Sanford discloses everything as applied above (see claim 1), in addition Sanford discloses wherein the second drive transistor is connected between the power supply line and the anode of the display element. Specifically Sanford discloses that the second drive transistor Q302 is connected between the power supply line and the anode of the OLED 320 exhibited in figure 3.

Regarding claim 5, Sanford discloses everything as applied above (see claim 1), in addition Sanford discloses that the gate of the first drive transistor is coupled to a

data signal line through an address transistor. Specifically Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 5, Sanford discloses everything as applied above (see claim 2), in addition Sanford discloses that the gate of the first drive transistor is coupled to a data signal line through an address transistor. Specifically Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford in view of Koyama et al. (United States Patent Application Publication 2001/0043168), hereinafter referenced as Koyama.

Regarding claim 3, Sanford discloses everything as applied above (see claim 1), however Sanford fails to disclose wherein the second drive transistor is connected between a second power supply line and the anode of the display element, however the examiner maintains that it was well known in the art to provide wherein the second drive

transistor is connected between a second power supply line and the anode of the display element, as taught by Koyama.

In a similar field of invention Koyama discloses a display device. Further Koyama discloses that a second drive transistor 4406 is connected between a second power supply line VY1 and the anode of the display element 4414 disclosed in paragraph 131 and in paragraph 133 and in paragraph 149 and exhibited in figure 2.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford with Koyama by specifically providing wherein the second drive transistor is connected between a second power supply line and the anode of the display element for the purpose of allowing each pixel to use multiple power lines to decrease the length of power lines required for the display.

Regarding claim 4, Sanford and Koyama, the combination discloses everything as applied above (see claim 3), further Koyama discloses wherein the second power supply line is shared between pixels in a row of the array, hence the examiner maintains that it was well known in the art.

In a similar field of invention Koyama discloses a display device. Further Koyama discloses that a second drive transistor 4406 is connected between a second power supply line VY1 and the anode of the display element 4414 where the second power supply line is shared between a row of pixels disclosed in paragraph 149 and exhibited in figure 2.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford with Koyama by specifically providing wherein the second power supply line is shared between pixels in a row of the array for the purpose of allowing each pixel to use multiple power lines to decrease the length of power lines required for the display

Regarding claim 5, Sanford and Koyama, the combination discloses everything as applied above (see claim 3), in addition Sanford discloses that the gate of the first drive transistor is coupled to a data signal line through an address transistor. Specifically Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 5, Sanford and Koyama, the combination discloses everything as applied above (see claim 4), in addition Sanford discloses that the gate of the first drive transistor is coupled to a data signal line through an address transistor. Specifically Sanford discloses that the gate of the first drive transistor Q303 is coupled to data line 340 through address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 10-67.

Regarding claim 6, Sanford and Koyama, the combination discloses everything as applied above (see claim 5), further Koyama discloses wherein the data signal line comprises a column conductor shared between pixels in a column of the array, hence the examiner maintains that it was well known in the art.

In a similar field of invention Koyama discloses a display device. Further Koyama discloses that the data signal line Sn is a column conductor shared between the pixels of a column of the array of pixels disclosed in paragraph 149 and exhibited in figure 2.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford with Koyama by specifically providing wherein the data signal line comprises a column conductor shared between pixels in a column of the array for the purpose of allowing the pixels to be arranged in rows and columns to display an image.

Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanford in view of Shimoda (United States Patent 6,809,706), hereinafter referenced as Shimoda.

Regarding claim 9, Sanford discloses a method of driving the pixels of an active matrix electroluminescent display device comprising an array of display pixels each having an electroluminescent display element, the method comprising: holding the voltage across the display element by applying a holding voltage through a first amorphous silicon or microcrystalline silicon NMOS transistor; while holding the voltage across the display element, storing a desired gate-source voltage on a storage capacitor connected between the gate and source of the second transistor, the gate-source voltage corresponding to a desired source-drain current for driving the display element; removing the holding voltage from the display element; and driving the desired source-drain current through the electroluminescent display element. Specifically

Sanford discloses a method for driving an EL display with pixels with EL display elements comprising:

holding the voltage across an OLED 320 by applying a voltage through a first amorphous silicon NMOS transistor Q302 disclosed in column 6 lines 16-35 and exhibited in figure 3.

storing a desired gate-source voltage on a storage capacitor Cs310 connected between the gate and source of the second transistor Q303, the gate-source voltage corresponding to a desired source-drain current for driving the OLED 320 disclosed in column 6 lines 16-67 and exhibited in figure 3.

removing the voltage from the OLED 320 disclosed in column 6 lines 30-35.

driving the desired source-drain current through the OLED 320 disclosed in column 6 lines 41-48, however Sanford fails to disclose the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor, however the examiner maintains that it was well known in the art to provide the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor, as taught by Shimoda.

In a similar field of invention Shimoda discloses a drive circuit for a display device. Shimoda further discloses that a voltage supplied from a transistor Tr1 to a capacitor C1 holds the gate-source voltage of a second NMOS transistor Tr2 exhibited in figure 12A and disclosed in column 4 lines 19-20 and in column 7 lines 61-64.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sanford with Shimoda by specifically providing the holding voltage holding the source voltage of a second amorphous silicon or microcrystalline silicon NMOS transistor for the purpose of allowing the OLED to display a portion of an image properly.

Regarding claim 10, Sanford and Shimoda, the combination discloses everything as applied above (see claim 9), further Sanford discloses wherein the desired source-drain current is driven through the second transistor by applying a first power supply voltage to the second transistor. Specifically Sanford discloses that the desired source-drain current is driven through the second transistor Q303 by applying a first power supply voltage Vdd to the transistor disclosed in column 6 lines 34-48.

Regarding claim 11, Sanford and Shimoda, the combination discloses everything as applied above (see claim 10), further Sanford discloses wherein the first power supply voltage is not applied to the second transistor while the voltage across the display element is held. Specifically Sanford discloses that the first power supply voltage Vdd is not applied to the second transistor Q303 while the voltage across the OLED is held constant disclosed in column 6 lines 30-34.

Regarding claim 12, Sanford and Shimoda, the combination discloses everything as applied above (see claim 11), further Sanford discloses wherein the first power supply voltage and the holding voltage are provided by a shared power supply line. Specifically Sanford discloses that first power supply voltage and the holding voltage on

the capacitor Cs310 are provided by a shared power supply line Vdd exhibited in figure 3 and disclosed in column 6 lines 34-38 and in column 4 lines 58-62.

Regarding claim 13, Sanford and Shimoda, the combination discloses everything as applied above (see claim 9), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 13, Sanford and Shimoda, the combination discloses everything as applied above (see claim 10), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 13, Sanford and Shimoda, the combination discloses everything as applied above (see claim 11), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done

by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Regarding claim 13, Sanford and Shimoda, the combination discloses everything as applied above (see claim 12), further Sanford discloses wherein storing a desired gate-source voltage on a storage capacitor comprises coupling data from a data signal line to the storage capacitor through an address transistor. Specifically Sanford discloses that storing a desired gate-source voltage on storage capacitor Cs310 is done by coupling data from a data signal line 340 to the storage capacitor Cs310 through an address transistor Q301 exhibited in figure 3 and disclosed in column 6 lines 16-40.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is (571)270-3568. The examiner can normally be reached on Monday-Friday (7:30-5:00 EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jefferey Harold can be reached on 571-272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stuart McCommas
Examiner
Art Unit 4115

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/Jefferey F Harold/
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